REMARKS

In accordance with the foregoing, claims 1, 4, 5, 7, and 8 have been amended. No claims have been cancelled and new claims 9 and 10 have been added. Claims 1-10 are pending and under consideration.

No new matter is being presented, and approval and entry of the foregoing amendments and new claims are respectfully requested.

REJECTION UNDER 35 U.S.C. §102(b):

In the Office Action at pages 2-3, the Examiner rejects claims 1-5 and 7 under 35 U.S.C. §102(b) in view of Takaba et al (U.S. Patent No. 5,565,856) (hereinafter "Takaba"). This rejection is respectfully traversed and reconsideration is requested.

"Anticipation requires the presence in a single prior art reference of the disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GMBH v. American Hoise and Derrick Co., 221 USPQ 481, 485 (Fed. Cir 1984). The Patent Office has the burden of making out a prima facie case, which requires it to produce the factual basis for its rejection in an application under §§102 and 103. In re Warner, 154 USPQ 173, 177 (CCPA 1967).

Claim 1

Claim 1 has been amended to recite "wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus." As argued previously, the abnormality detection device is independent of a CPU controlling the communication bus, and detects the abnormality directly from the communication bus, without CPU or software intervention. According to the present invention as recited in claim 1, it is possible to detect the abnormality in the communication bus with a high reliability even under complex conditions, without increasing the load on the CPU or software. Takaba fails to teach or even suggest, among other features, these features of the claimed invention. As shown in Fig. 24 of Takaba, the time lapse measuring device 945 is located within the CPU 110, thus requiring CPU or software intervention to measure the time lapse (emphasis added). Therefore, Takaba does not teach or suggest detecting the abnormality directly from the communication bus, without CPU or software intervention.

Additionally, the Examiner asserts that the claimed comparator is taught in column 6, lines 4-16 of Takaba, and that the abnormality detection device independent of a CPU

controlling the communication bus is taught in Fig. 1(a), element 300, of Takaba. The Applicant respectfully disagrees with this assertion. The diagnosis unit 300 and the CPU 110 shown in Fig. 1(a) of Takaba are connected via the bus 400. CPU 110 is provided within the controller 100 that is connected to the diagnosis unit 300 via the bus 400. As such, the diagnosis unit 300 is not related to the abnormality detection device. Furthermore, Fig. 24, column 7, lines 64-67, and column 8, lines 1-24 of Takaba, which were relied on by the Examiner in support of the rejection, clearly show that the communication abnormality determining device 840, including the time lapse measuring device 925, is included in the CPU 110 and not in the diagnosis unit 300. This further supports the fact that the diagnosis unit 300 does not have any relation to detecting the abnormality. As such, it makes no difference if the diagnosis unit 300 is independent of the CPU 110 because the diagnosis unit 300 does not perform the abnormality detection as recited in claim 1.

Takaba further explicitly states that "[d]iagnosis unit 300 can be connected, when diagnosis is necessary, through bus 400 to controllers 100 and 200 thus permitting readout of, for example, abnormality detection data processed by the controllers 100 and 200" (emphasis added). This clearly states that abnormality detection is performed by the controllers 100 and 200, not the diagnosis unit 300. Accordingly, it is impossible for the abnormality detection to occur independent of the CPU because the controllers are a part of the CPU. Therefore, Takaba fails to teach or suggest "wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus" as recited in claim 1.

Amended claim 1 further recites "a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level." The Examiner asserts that the timer counter is taught in Takaba and cites Fig. 9 element 825, Fig. 24 element 945, column 7, lines 64-67 and column 8, lines 1-23. It is respectfully submitted that this feature is neither taught nor suggested by Takaba.

The time lapse measuring device 945 shown in Fig. 9 measures the time it takes for the data transmitted to the communication IC 140 to be transferred to the bus 400 via the driver/receiver 145, as described in column 7, lines 51-53. The ABSY signal is set to a high level in a state where the data is input to the communication IC 140, and the ABSY signal is set to a low level in a state where no data is input to the communication IC 140, as described in column 8, lines 25-30 and column 6, lines 4-16. An abnormality is detected if the data remains in the communication IC 140 after a predetermined time. Therefore, Takaba shows measuring

the amount of time that data remains in the communication IC and does not measure the time which a logical level output remains on the communication bus. Measuring the amount of time data is stored in an IC and the amount of time that a logic level is sustained on a bus is not the same function. Takaba does not detect an abnormality on the communication bus as recited in the claim. As such, contrary to the Examiner's assertions, Takaba fails to teach or even suggest "a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level."

Additionally, as discussed above, the time lapse measuring device of Takaba is provided within the CPU and requires the use of software to measure time. Therefore, Takaba does not disclose detecting the abnormality directly from the communication bus, without software intervention. For at least the above reasons, it is respectfully submitted that Takaba does not show the features of claim 1 and claim 1 is patentable over the prior art.

Claim 5

Claim 5 recites "at least two timer counters each configured to measure a time during which a signal transmitted through the communication bus continues to be a first logical level." The Examiner asserts that the additional timer is described in column 1, lines 50-56 of Takaba. The Applicant respectfully submits that Takaba does not disclose this claimed feature.

Takaba merely shows a buffer that stores the status of the data at a first time. This buffer does not perform any type of measurement or counting as recited in the claimed features. Merely storing the status of data at a first time does not make the buffer the second timer. Storing timing data and actually performing a time measurement or counting are entirely different processes. Takaba clearly states that the buffer "stores the data to be transmitted to the diagnosis unit" (column 1, lines 52-53). The buffer of Takaba stores timing data after the data has been determined, and does not perform the time measurement (emphasis added). As such, the buffer of Takaba is not a second timer as asserted by the Examiner. Therefore, Takaba fails to show or even suggest "at least two timer counters each configured to measure a time during which a signal transmitted through the communication bus continues to be a first logical level."

Claim 5 additionally recites "a register configured to cumulatively add the time measured by at least one of said at least two timer counter, the register being initialized at predetermined intervals." The Examiner asserts that the register for adding the time measured by one of the timers is described in column 7, lines 40-45 of Takaba. The Applicant respectfully submits that Takaba does not show this claimed feature.

In column 7, lines 40-45, Takaba merely shows counting data bytes and not "the time measured by at least on of said at least two timer counters." As described in column 7, lines 31-37, the "variable k" is used to represent the detection of the change in a logic level. This variable does not add time measured by a timer. The "variable k" of Takaba detects the change in logic at a certain timing, but does not actually increment time measured by a timer. Therefore, Takaba fails to show or even suggest "a register configured to cumulatively add the time measured by at least one of said at least two timer counter, the register being initialized at predetermined intervals."

As such, at least for the reasons stated above and the arguments regarding claim 1 that similarly apply, it is respectfully submitted that Takaba does not show the features of claim 5 and claim 5 is patentable over the prior art.

Claim 7

Claim 7 as amended recites:

> a CPU configured to control the communication bus;
>
> a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level; and
>
> a comparator configured to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the timer counter and the comparator are independent of the CPU and are operatively coupled to detect the abnormality directly from the communication bus.

Therefore, it is submitted that claim 7 patentably distinguishes over the prior art.

Claims 2-4

Claims 2-4 depend directly from claim 1 and include all of the features of that claim plus additional features which distinguish over the prior art. Therefore, it is submitted that claims 2-4 are patentably distinguishable over the prior art.

ALLOWABLE SUBJECT MATTER

On page 3 of the present Office Action, the Examiner indicates that claim 6 contains allowable subject matter and would be allowable if rewritten in independent form including all of the limitations of the base claim. Claim 6 is directly dependent upon claim 5. Since the Applicant respectfully submits that claim 5 is patentably distinguishable over the prior art, as discussed above, it is submitted that claim 6 is patentable at least due to its dependence from claim 5.

On page 8, independent claim 8 has been indicated as allowable. Claim 8 is amended, however, in order to improve the form as shown in the proposed Amendment. It is respectfully submitted that the allowability of claim 8 remains unchanged by the amendment.

PATENTABILITY OF NEW CLAIMS:

New claims 9 and 10 depend from claims 1 and 5, respectively, and include all of the features of the base claim plus additional features which distinguish over the prior art. Claims 9 and 10 further recite that the abnormality detection device "detects the abnormality directly from the communication bus by hardware." Therefore, Claims 9 and 10 are deemed patentable due at least to their depending from independent claims 1 and 5.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. And further, it is respectfully submitted that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: 3-2-06

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